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EXAMINER	
CRAWFORD, LATANYA N	
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2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/557,746	SHIBATA, SATOSHI	
	Examiner	Art Unit	
	LATANYA CRAWFORD	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *1-4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/01/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the correspondence filed on 10/01/2008. Currently, claims 5-17 are pending. Claims 1-4 have been cancelled.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 5, 9, & 13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The Examiner notes that the recitation of: by heat treating the amorphous layer at a prescribed temperature, having the previous amended portion, "without implanting ions into the amorphous layer" as applied to claims 5, 9, & 13 is not properly described in the application where mentioned [0055-0056], [0060],[0072], & [0097]. The limitation "without implanting ions…" is a negative limitation. Negative limitations must find positive support in the specification. The Examiner takes the position that the limitation of: by heat treating the amorphous layer at a prescribed temperature "without implanting ions into the amorphous layer" to mean that the ion implantation occurs prior to or after the heat treating of the amorphous layer and not during or simultaneously with the heat treating process.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 5 is rejected under 35 U SC 102(e) as being anticipated by Paton (US Patent 7,091,097 B1).

Regarding claim 5, Paton et al. discloses forming an amorphous layer (50) in a region from a surface of a semiconductor region (10) of a first conductivity type (inherent that the substrate is doped with a first conductivity) to a first depth (column 5, lines 10-24); by heat treating the amorphous layer (50) at a prescribed temperature without implanting ions into the amorphous layer restoring a crystal structure of the amorphous layer (50) in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth (column 5, lines 45-56) fig. fig. 2c; after the heat treating, forming a first impurity layer (30) of a second conductivity type which has pn junction at a third depth that is shallower than the second depth by introducing ions into the heat treated amorphous layer (50') (column 6, lines 17-21); activating the first impurity layer (column 6, lines 17-31; column 4, lines 20-33).

6. Claims 5-6 are rejected under 35 U SC 102(e) as being anticipated by Keys (US Pub no. 2004/0235280 A1)

Regarding claim 5, Keys et al. discloses forming an amorphous layer (202) in a region from a surface of a semiconductor region of a first conductivity type to a first depth[0020]; by heat treating the amorphous layer at a prescribed temperature without implanting ions into the amorphous layer[0028], restoring a crystal structure of the amorphous layer (202) in a region from the first depth (211) to a second depth (202) that is shallower than the first depth so that the amorphous layer shrinks to the second depth [0020] ;[0034]; [0035]; after the heat treating, forming a first impurity layer of a second conductivity type which has pn junction at a third depth that is shallower than the second depth by introducing ions into the heat treated amorphous layer [0020]; [0028]; [0036]; activating the first impurity layer [0037].

Regarding claim 6, Keys et al. discloses the third depth is in a range of 5 nm to 15 nm [0031].

7. Claims 13 & 15 are rejected under 35 U SC 102(e) as being anticipated by Keys (US Pub no. 2004/0235280 A1).

Regarding claim 13, Keys et al. discloses forming a gate electrode (508) on a semiconductor region (502) of a first conductivity type [0039]; forming an amorphous layer in a region from a surface of the semiconductor region to a first depth [0040]; forming an insulating sidewall (514 /516) on a side surface

of the gate electrode (508) while restoring a crystal structure [0042] of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth [0020] ;[0034]; [0035], the restoration of the crystal structure of the amorphous layer being caused by heat treatment of a prescribed temperature which is conducted during formation of the sidewall without implanting ions into the amorphous layer [0042]; after the heat treating, forming a first impurity layer of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions [0020]; [0028]; [0036] on both sides of the gate electrode (508) in the heat treated amorphous layer [0043]; activating the first impurity layer [0037].

Regarding claim 15, Keys et al. discloses the third depth is in a range of 5 nm to 15 nm [0031].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 6 is rejected under 35 U.S.C 103 (a) as being unpatentable in view of Paton (US Patent 7,091,097 B1) in view of Keys (US Pub no. 2004/0235280 A1).

Regarding claim 6, Paton et al. discloses all the claim limitations of claim 5 but fails to teach the third depth is in a range of 5 nm to 15 nm.

However, Keys et al. discloses the third depth is in a range of 5 nm to 15 nm [0031]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Paton et al. with the third depth is in a range of 5 nm to 15 nm taught by Keys et al. since doing so would provide shallow S/D regions.

10. Claim 7 is rejected under 35 U.S.C 103 (a) as being unpatentable in view of Paton (US Patent 7,091,097 B1) in view of Yu (US Patent 6,521,502 B1).

Regarding claim 7, Paton et al. discloses all the claim limitations of claim 5 and further teaches the prescribed temperature is in the range of 475°C to 600°C (column 5, lines 60-65) but fails to disclose the activation temperature range of 500°C to 700° C.

However, Yu et al. discloses the activation temperature range of 500°C to 700 °C (column 6, lines 64-67). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of Paton et al. with the activation temperature range of 500°C to 700 °C taught by Yu et al. since doing so would form steep junctions, which is desirable for transistors with small dimensions.

11. Claim 8 is rejected under 35 U.S.C 103 (a) as being unpatentable in view of Paton (US Patent 7,091,097 B1) in view of Wu (US Patent 6,391,751).

Regarding claim 8, Paton et al. discloses all the claim limitations of claim 5 but fails to teach that the gate electrode is formed is non-uniformly formed distributed on the semiconductor region.

However, Wu et al discloses a pattern of a gate electrode 56 that is formed on the semiconductor region 50 is non-uniformly distributed on the semiconductor region 50 (fig. 1a & 1b; column 1, lines 51-52). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of Paton et al. with the gate electrode formed non-uniformly on the semiconductor device taught by Wu et al. since doing so would provide increased surface area.

12. Claims 13 & 15 are rejected under 35 U.S.C 103 (a) as being unpatentable in view of Paton (US Patent 7,091,097 B1) in view of Keys (US Pub no. 2004/0235280 A1).

Regarding claim 13, Paton et al. discloses forming a gate electrode (24) on a semiconductor region (10) of a first conductivity type (inherent that the substrate is doped with a first conductivity) (column 4, lines 48-49); forming an amorphous layer (50) in a region from a surface of the semiconductor region (10) to a first depth (column 5, lines 10-24); forming an insulating sidewall (26) on a side surface of the gate electrode (24) (column 4, lines 50-53) while restoring a crystal structure of the amorphous layer (50) in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth (column 5, lines 45-56) fig. fig. 2c; after the heat

treating, forming a first impurity layer (30) of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions on both sides of the gate electrode (24) in the heat treated amorphous layer (50') (column 6, lines 17-21; column 4, lines 54-56); activating the first impurity layer (column 6, lines 17-31; column 4, lines 20-33). Paton further teaches the restoration of the crystal structure of the amorphous layer (50) being caused by heat treatment of a prescribed temperature without implanting ions into the amorphous layer (50) (column 5, lines 45-56; column 4, lines 20-33) fig. fig. 2c but fails to teach that the restoration is conducted during formation of the sidewall.

However, Key et al. teaches the restoration is conducted during formation of the sidewall [0042]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Paton et al. with conducting the crystal restoration during the formation of the sidewall taught by Keys et al. since doing so would reduce processing steps.

Regarding claim 15, Keys et al. discloses the third depth is in a range of 5 nm to 15 nm [0031].

13. Claims 14 & 16 are rejected under 35 U.S.C 103 (a) as being unpatentable in view of Paton (US Patent 7,091,097 B1) in view of Keys (US Pub no. 2004/0235280 A1) as applied to claim 13, and further in view of Yu (US Patent 6,521,502 B1).

Regarding claim 14, Paton et al. as modified by Keys et al. discloses all the claim limitations of claim 13 but fails to disclose after the step of forming the first impurity layer, forming a second impurity layer of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer, wherein the second impurity layer is simultaneously activated in the step of activating the first impurity layer.

However, Yu et al. discloses after the step of forming the first impurity layer 20 & 22 (40 & 42), forming a second impurity layer 50 & 52 of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer (fig. 4; column 6, lines 8-14 & 16-18), wherein the second impurity layer is simultaneously activated in the step of activating the first impurity layer (column 7, lines 1-6). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of Paton et al. & Keys et al. with the of Yu et al. since doing so would form steep junctions, which is desirable for transistors with small dimensions.

Regarding claim 16, Paton et al. teaches the prescribed temperature is in the range of 475°C to 600°C (column 5, lines 60-65). Yu et al. discloses the activation temperature range of 500°C to 700 °C (column 6, lines 64-67).

14. Claim 17 is rejected under 35 U.S.C 103 (a) as being unpatentable in view of Paton (US Patent 7,091,097 B1) in view of Keys (US Pub no. 2004/0235280 A1) as applied to claim 13, and further in view of Wu (US Patent 6,391,751).

Regarding claim 17, Paton et al. as modified by Keys et al. discloses all the claim limitations of claim 13 but fails to teach that the gate electrode is formed is non-uniformly formed distributed on the semiconductor region.

However, Wu et al discloses a pattern of a gate electrode 56 that is formed on the semiconductor region 50 is non-uniformly distributed on the semiconductor region 50 (fig. 1a & 1b; column 1, lines 51-52). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of Paton et al. & Keys et al. with the gate electrode formed non-uniformly on the semiconductor device taught by Wu et al. since doing so would provide increased surface area.

15. Claims 8 & 17 are rejected under 35 U.S.C 103 (a) as being unpatentable in view of Keys (US Pub no. 2004/0235280 A1) in view of Wu (US Patent 6,391,751).

Regarding claim 8, Keys et al discloses the limitations of claim 5 and further teaches a gate electrode 508 that is formed on a semiconductor region 502 but fails to teach that the gate electrode is formed is non-uniformly formed distributed on the semiconductor region.

However, Wu et al discloses a pattern of a gate electrode 56 that is formed on the semiconductor region 50 is non-uniformly distributed on the semiconductor region 50 (fig. 1a & 1b; column 1, lines 51-52). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of Keys et al. with the gate electrode formed non-uniformly on the semiconductor device taught by Wu et al. since doing so would provide increased surface area.

Regarding claim 17, Wu et al discloses a pattern of a gate electrode 56 that is formed on the semiconductor region 50 is non-uniformly distributed on the semiconductor region 50 (fig. la & lb; column 1, lines 51-52).

16. Claims 7, 14, 16 are rejected under 35 U.S.C 103 (a) as being unpatentable in view of Keys (US Pub no. 200410235280 A1) in view of Yu (US Patent 6,521,502 B1).

Regarding claim 7, Keys et al. discloses all the claim limitations of 5 and further teaches the prescribed temperature is in the range of 475°C to 600°C [0028]; [0036]; [0042] but fails to disclose the activation temperature range of 500°C to 700° C.

However, Yu et al. discloses the activation temperature range of 500°C to 700 °C (column 6, lines 64-67). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of Keys et al. with the activation

temperature range of 500°C to 700 °C taught by Yu et al. since doing so would form steep junctions, which is desirable for transistors with small dimensions.

Regarding claim 14, Keys et al. discloses all the claim limitations of 13 and further teaches the prescribed temperature is in the range of 475°C to 600°C [0028];[0036]; [0042].Yu et al. discloses after the step of forming the first impurity layer 20 & 22 (40 & 42), forming a second impurity layer 50 & 52 of a first conductivity type which has a pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions on both sides of the gate electrode in the amorphous layer (fig. 4; column 6, lines 8-14 & 16-18), wherein the second impurity layer is simultaneously activated in the step of activating the first impurity layer (column 7, lines 1-6).

Regarding claim 16, Keys et al. discloses all the claim limitations of 13 and further teaches the prescribed temperature is in the range of 475°C to 600°C [0028]; [0036]; [0042]. Yu et al. discloses the activation temperature range of 500°C to 700 °C (column 6, lines 64-67).

17. Claims 9 & 11 are rejected under 35 U.S.C 103 (a) as being unpatentable in view of Paton (US Patent 7,091,097 B1) in view of Yu (US Patent 6,521,502 B1).

Regarding claim 9, Paton et al. discloses forming an amorphous layer (50) in a region from a surface of a semiconductor region (10) of a first conductivity type (inherent that the substrate is doped with a first conductivity) to a first depth

(column 5, lines 10-24); by heat treating the amorphous layer (50) at a prescribed temperature without implanting ions into the amorphous layer restoring a crystal structure of the amorphous layer (50) in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth (column 5, lines 45-56) fig. fig. 2c; after the heat treating, forming a first impurity layer (30) of a second conductivity type which has pn junction at a third depth that is shallower than the second depth by introducing ions into the heat treated amorphous layer (50') (column 6, lines 17-21); after the heat treating, forming a second impurity layer (40) (column 6, lines 17-31; column 4, lines 20-33) but fails to teach the conductivity type of the second impurity layer of a first conductivity which has pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions into the heat treated amorphous layer; and activating the first impurity layer and the second impurity layer.

However, Yu et al. teaches second impurity layer of a first conductivity which has pn junction 50 & 52 at a level that is shallower than the first depth and deeper than the third depth by introducing ions into the heat treated amorphous layer (fig. 4; column 6, lines 8-14); and activating the first impurity layer and the second impurity layer (column 7, lines 1-6). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of Paton et al. with teachings of Yu et al. since doing so would form junctions that are substantially defect-free.

Regarding claim 11, Yu et al. discloses the prescribed temperature is in a range of 475 °C to 600° C (column 6, lines 58-59), and the activation is conducted in a temperature range of 500° C to 700° C (column 6, lines 64-67).

18. Claim 10 is rejected under 35 U.S.C 103 (a) as being unpatentable in view of Paton (US Patent 7,091,097 B1) in view of Yu (US Patent 6,521,502 B1) as applied to claim 9, and further in view of Keys (US Pub no. 2004/0235280 A1).

Regarding claim 10, Paton et al. as modified by Yu et al. discloses all the claim limitations of claim 9 but fails to teach the third depth is in a range of 5 nm to 15 nm.

However, Keys et al. discloses the third depth is in a range of 5 nm to 15 nm [0031]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Paton et al. & Yu et al. with the third depth is in a range of 5 nm to 15 nm taught by Keys et al. since doing so would provide shallow S/D regions.

19. Claim 12 is rejected under 35 U.S.C 103 (a) as being unpatentable in view of Paton (US Patent 7,091,097 B1) in view of Yu (US Patent 6,521,502 B1) as applied to claim 9, and further in view of Wu (US Patent 6,391,751).

Regarding claim 12, Paton et al. as modified Yu et al. discloses all the claim limitations of claim 9 but fails to teach a pattern of a gate electrode that is formed on the semiconductor region is non-uniformly distributed on the semiconductor region.

However, Wu et al discloses a pattern of a gate electrode 56 that is formed on the semiconductor region 50 is non-uniformly distributed on the semiconductor region 50 (fig. 1a & 1b; column 1, lines 51-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of Paton et al. & Yu et al. with the gate electrode formed non-uniformly on the semiconductor device taught by Wu et al. since doing so would provide increased surface area.

20. Claims 9-11 are rejected under 35 U.S.C 103 (a) as being unpatentable in view of Keys (US Pub no. 2004/0235280 A1) in view of Yu (US Patent 6,521,502 B1).

Regarding claim 9, Keys et al. discloses forming an amorphous layer (202) in a region from a surface of a semiconductor region of a first conductivity type to a first depth[0020]; by heat treating the amorphous layer at a prescribed temperature without implanting ions into the amorphous layer[0028], restoring a crystal structure of the amorphous layer (202) in a region from the first depth (211) to a second depth (202) that is shallower than the first depth so that the amorphous layer shrinks to the second depth [0020] ;[0034]; [0035]; after the heat treating, forming a first impurity layer of a second conductivity type which has pn junction at a third depth that is shallower than the second depth by introducing ions into the heat treated amorphous layer [0020]; [0028]; [0036]; after the heat treating, forming a second impurity layer [0045] but fails to teach the conductivity type of the second impurity layer of a first conductivity which has

pn junction at a level that is shallower than the first depth and deeper than the third depth by introducing ions into the heat treated amorphous layer; and activating the first impurity layer and the second impurity layer.

However, Yu et al. teaches second impurity layer of a first conductivity which has pn junction 50 & 52 at a level that is shallower than the first depth and deeper than the third depth by introducing ions into the heat treated amorphous layer (fig. 4; column 6, lines 8-14); and activating the first impurity layer and the second impurity layer (column 7, lines 1-6). It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of Keys et al. with teachings of Yu et al. since doing so would form junctions that are substantially defect-free.

Regarding claim 10, Keys et al. discloses the third depth is in a range of 5 nm to 15 nm ([0031], lines 25-26).

Regarding claim 11, Yu et al. discloses the prescribed temperature is in a range of 475 °C to 600° C (column 6, lines 58-59), and the activation is conducted in a temperature range of 500° C to 700° C (column 6, lines 64-67).

21. Claim 12 is rejected under 35 U.S.C 103 (a) as being unpatentable in view of Keys(US Pub no. 2004/0235280 A1) in view of Yu (US Patent 6,521,502 B1) as applied to claim 9, and further in view of Wu (US Patent 6,391,751).

Regarding claim 12, Keys et al. as modified Yu et al. discloses all the claim limitations of claim 9 but fails to teach a pattern of a gate electrode that is

formed on the semiconductor region is non-uniformly distributed on the semiconductor region.

However, Wu et al discloses a pattern of a gate electrode 56 that is formed on the semiconductor region 50 is non-uniformly distributed on the semiconductor region 50 (fig. 1a & 1b; column 1, lines 51-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of manufacturing a semiconductor device of Keys et al. & Yu et al. with the gate electrode formed non-uniformly on the semiconductor device taught by Wu et al. since doing so would provide increased surface area.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LATANYA CRAWFORD whose telephone number is (571)270-3208. The examiner can normally be reached on Monday-Friday 7:30 AM -5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571)-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art Unit 2822

/LaTanya Crawford/
Examiner, Art Unit 2813